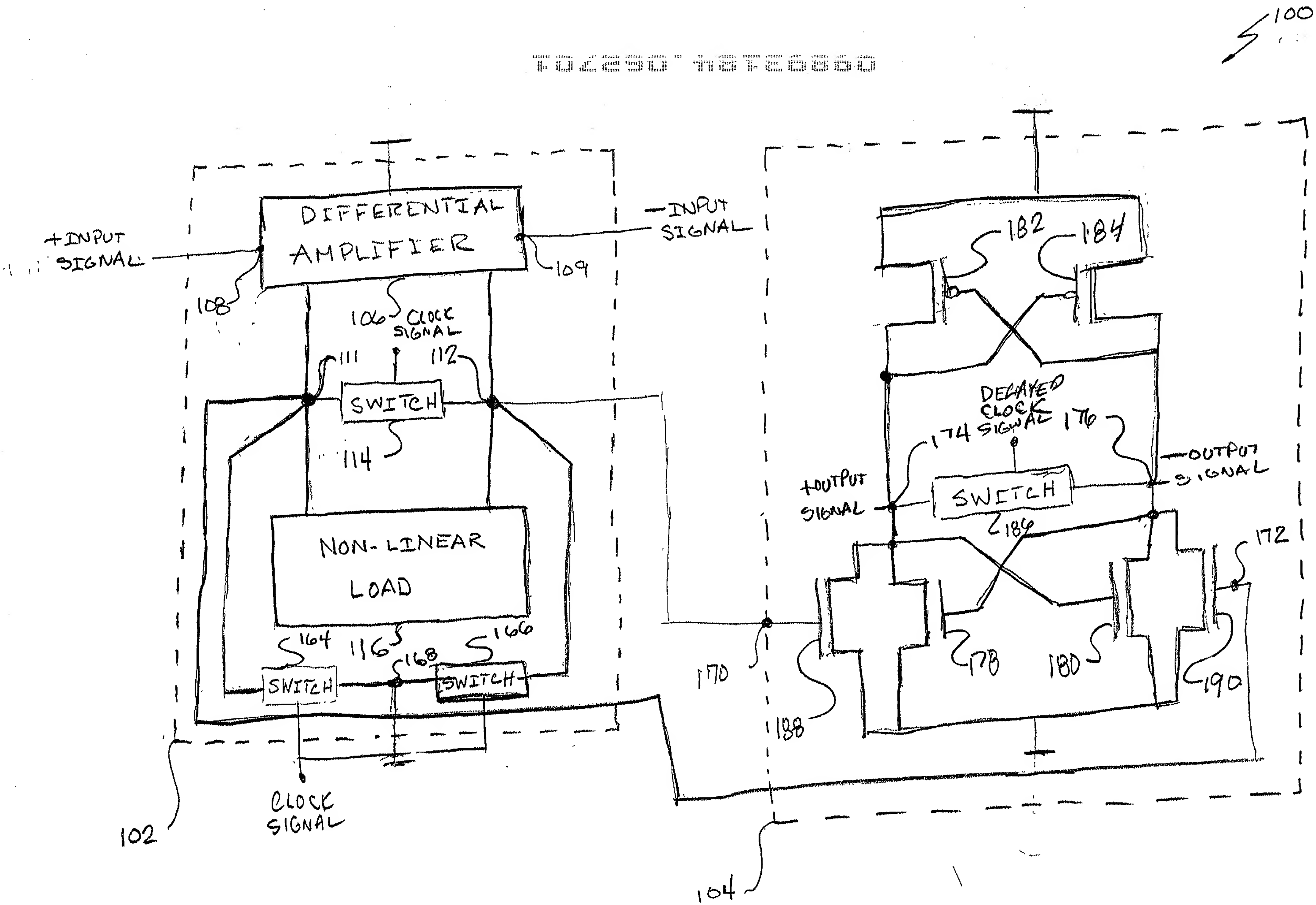
100
DIFFERENTIAL AMPLIFIER
+INPUT SIGNAL
-INPUT SIGNAL
108
109
106
CLOCK SIGNAL
111
112
SWITCH
114
NON-LINEAR LOAD
164
116
168
166
SWITCH
SWITCH
CLOCK SIGNAL
102
182
184
DELAYED CLOCK SIGNAL
174
176
+OUTPUT SIGNAL
-OUTPUT SIGNAL
SWITCH
186
172
170
178
180
190
188
104

Fig. 1A

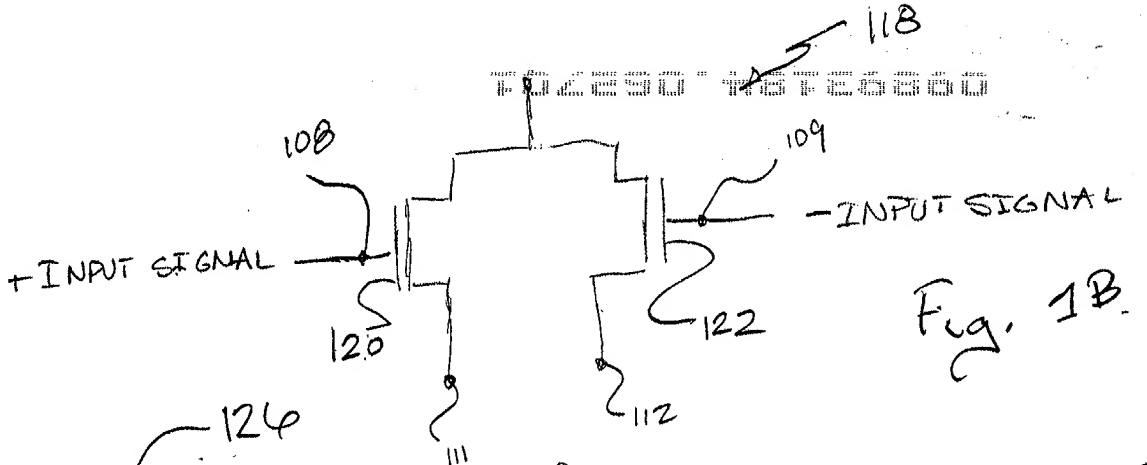
118
108
109
+INPUT SIGNAL
-INPUT SIGNAL
120
122
111
112

Fig. 1B

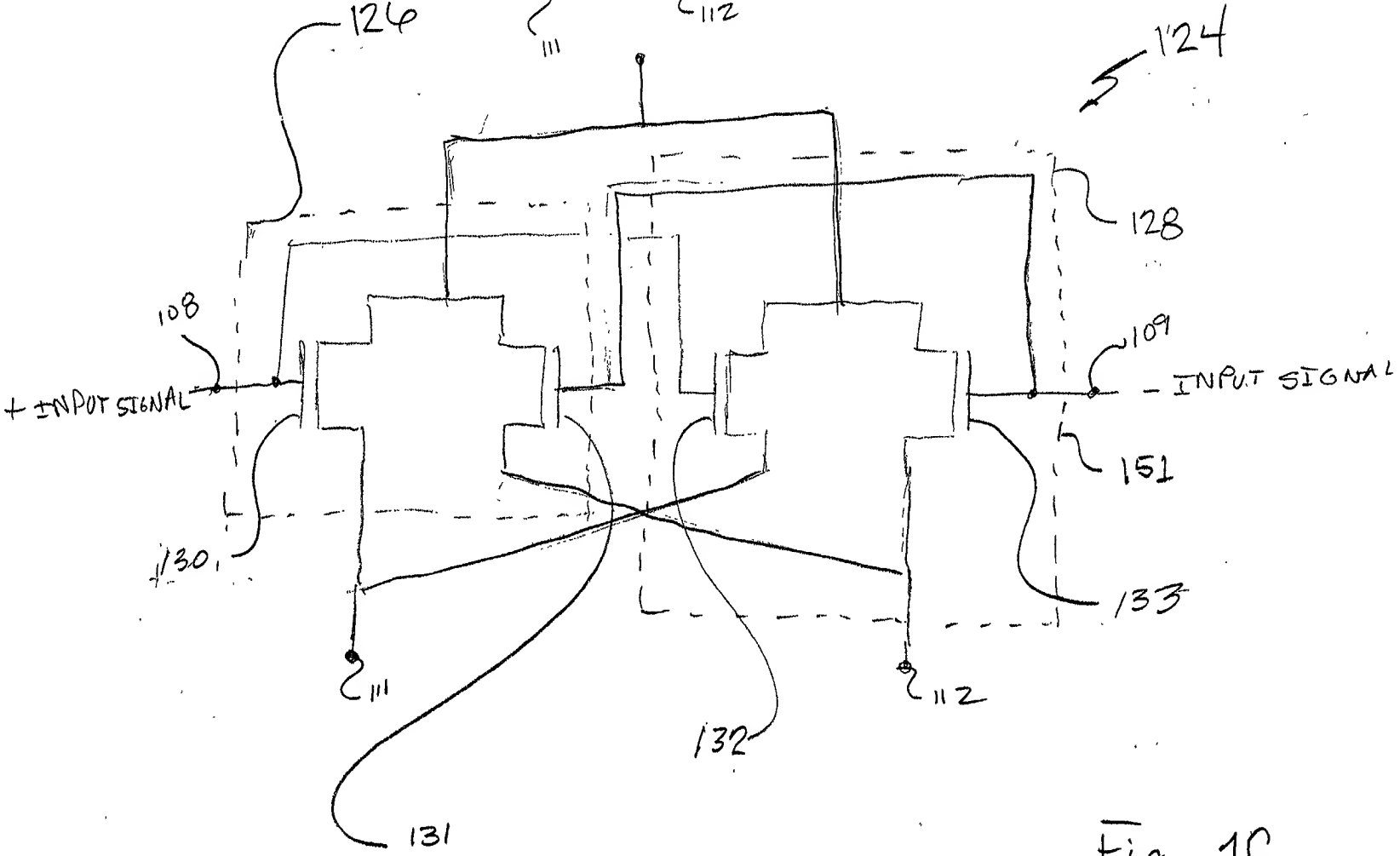
126
124
128
108
109
+INPUT SIGNAL
-INPUT SIGNAL
151
130
133
111
112
132
131

Fig. 1C

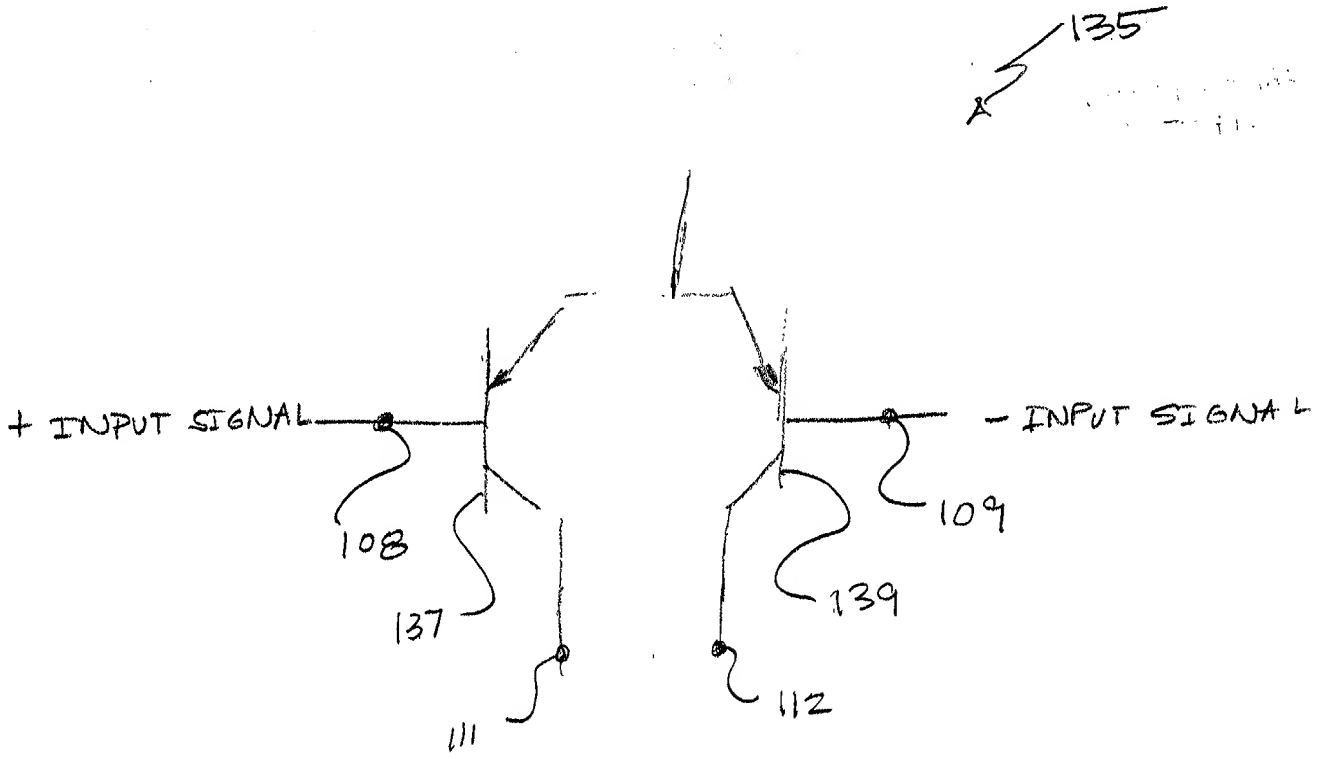

Fig. 1D

Fig. 1E

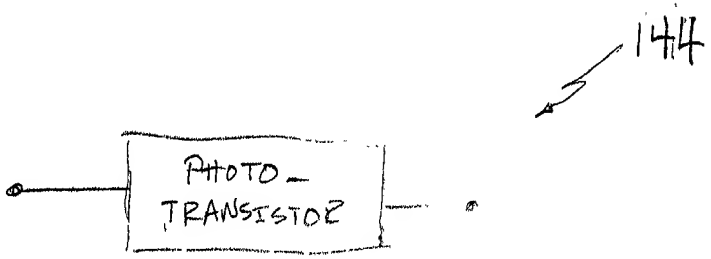

Fig. 1F

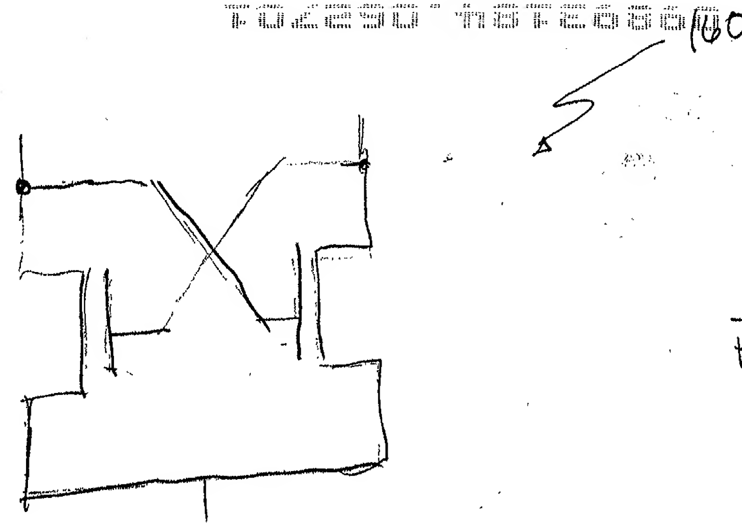

Fig. 1G

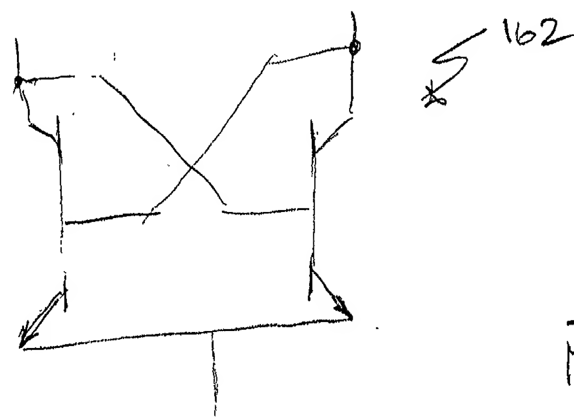

Fig. 1H

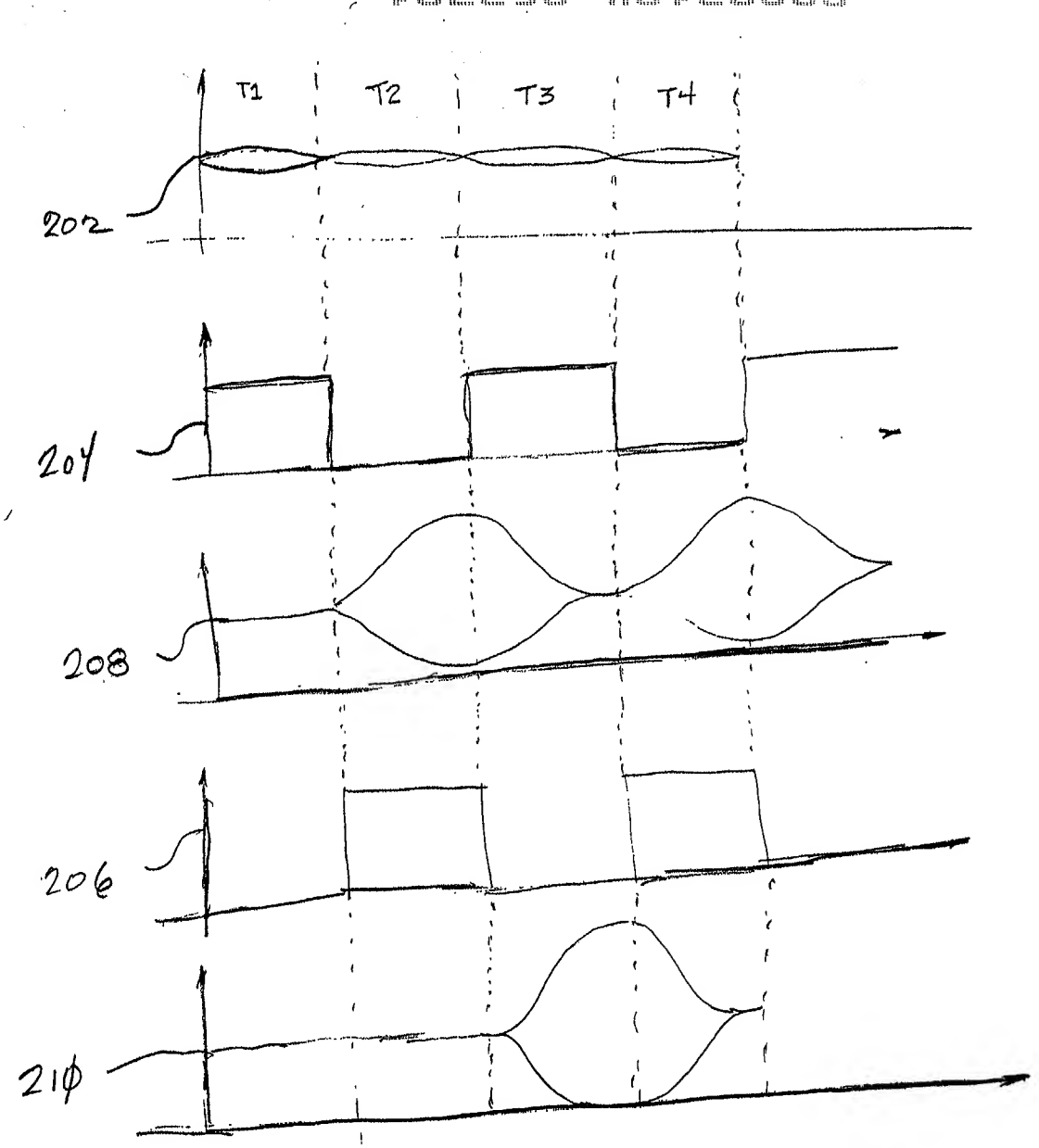

Fig. 2

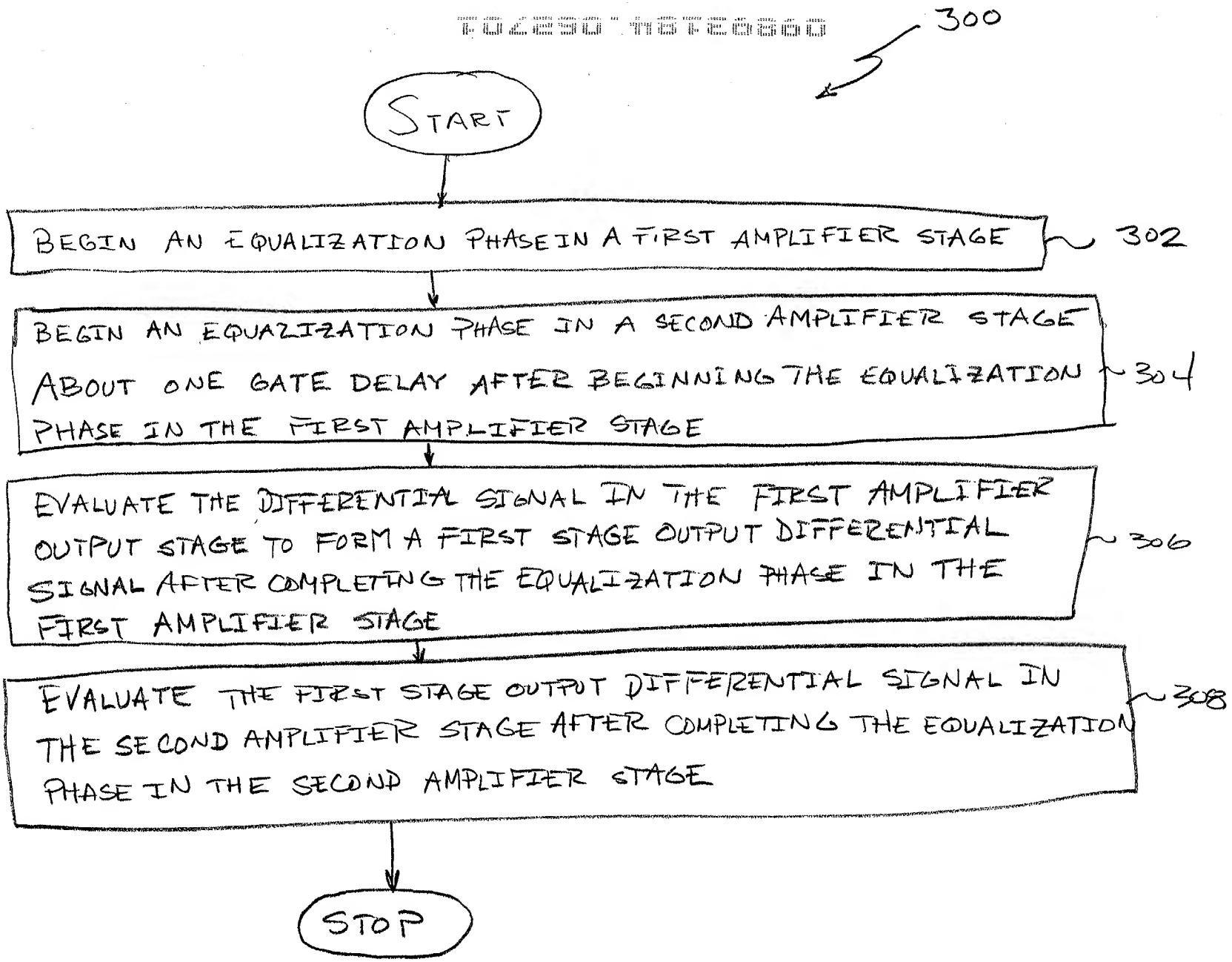
300
START
BEGIN AN EQUALIZATION PHASE IN A FIRST AMPLIFIER STAGE
302
BEGIN AN EQUALIZATION PHASE IN A SECOND AMPLIFIER STAGE ABOUT ONE GATE DELAY AFTER BEGINNING THE EQUALIZATION PHASE IN THE FIRST AMPLIFIER STAGE
304
EVALUATE THE DIFFERENTIAL SIGNAL IN THE FIRST AMPLIFIER OUTPUT STAGE TO FORM A FIRST STAGE OUTPUT DIFFERENTIAL SIGNAL AFTER COMPLETING THE EQUALIZATION PHASE IN THE FIRST AMPLIFIER STAGE
306
EVALUATE THE FIRST STAGE OUTPUT DIFFERENTIAL SIGNAL IN THE SECOND AMPLIFIER STAGE AFTER COMPLETING THE EQUALIZATION PHASE IN THE SECOND AMPLIFIER STAGE
308
STOP

Fig. 3

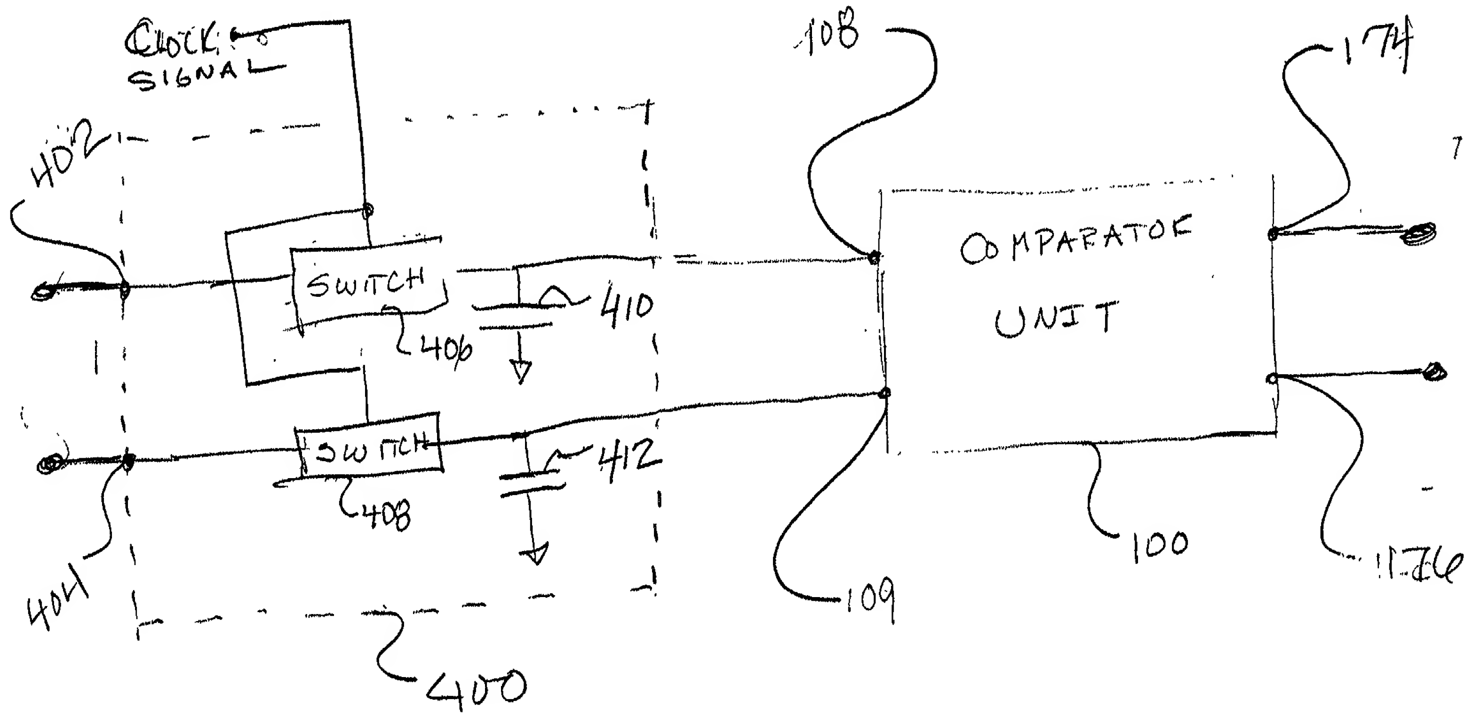
CLOCK SIGNAL
402
404
SWITCH
406
SWITCH
408
410
412
400
108
109
COMPARATOR UNIT
100
174
176

Fig. 4

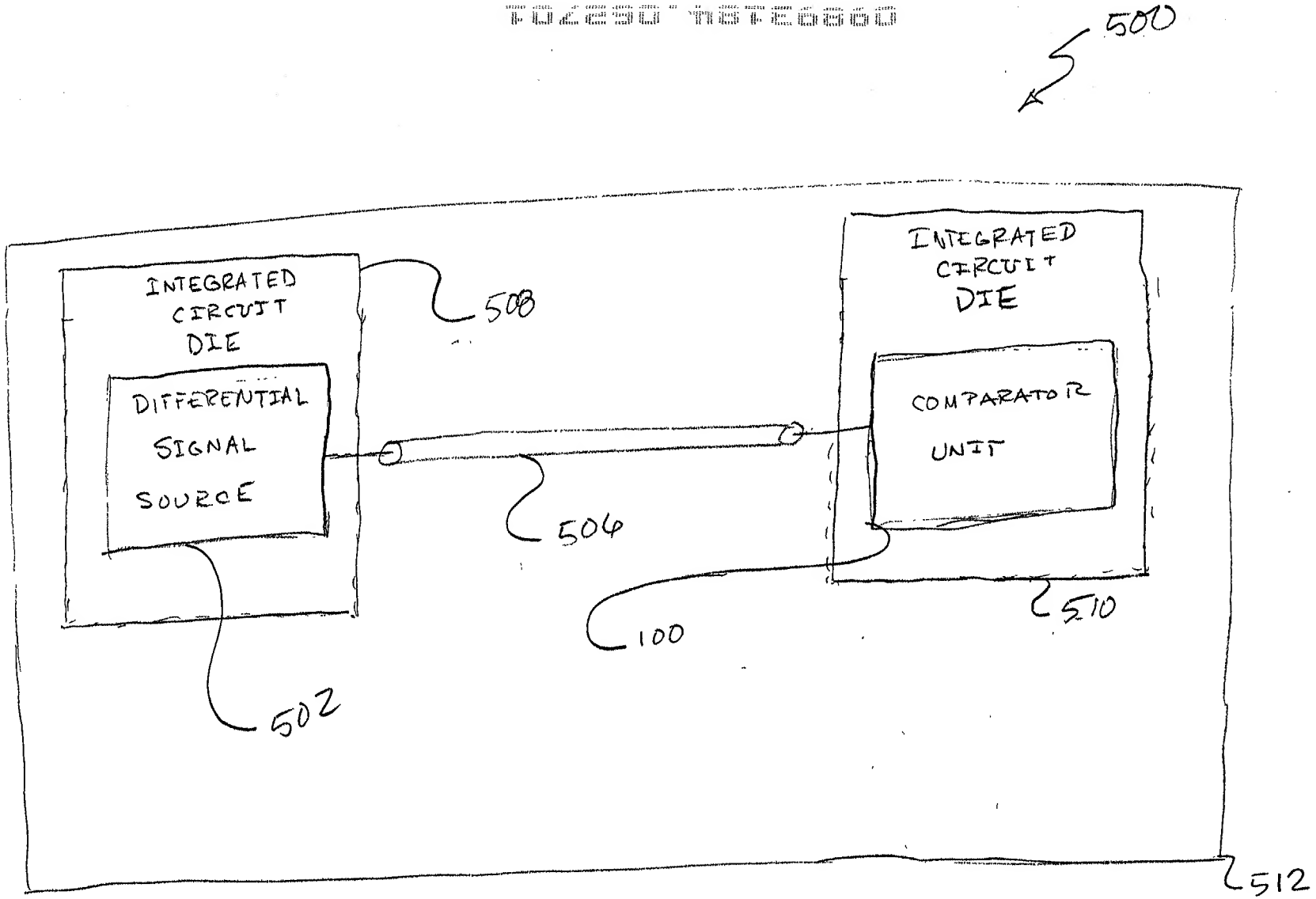

Fig. 5